In the Claims:

Please cancel claims 39 and 41. Please amend claim 40 to include the limitations of claim 39 and selected limitations of claim 23. Please amend claims 23-24 and 29-30 to correct typographical errors. The claims are as follows.

1-22. (Canceled)

23. (Currently amended) An electrical structure, ~~compising~~ comprising:

a semiconductor substrate having an electrically insulative isolation structure therein, wherein a top surface of the substrate and a top surface of the ~~insulation~~ isolation structure are coplanar;

a first gate oxide layer on the substrate and in direct mechanical contact with the top surface of the substrate;

a first polysilicon layer on the first gate oxide layer and in direct mechanical contact with the first gate oxide layer;

a second gate oxide layer on the isolation structure and in direct mechanical contact with the top surface of the isolation structure, wherein the first and second gate oxide layers have a same thickness in a first direction perpendicular to the top surface of the substrate, and wherein the first gate oxide layer ~~layer~~ has a smaller width than the second gate oxide layer in a second direction parallel to the top surface of the substrate; and

a second polysilicon layer on the second gate oxide layer and in direct mechanical contact with the second gate oxide layer, wherein the first polysilicon layer has a smaller thickness than the second polysilicon layer in the first direction, and wherein the first polysilicon layer has a

smaller width than the second polysilicon layer in the second direction.

24. (Currently amended) The electrical structure of claim 23, further comprising a first dielectric film surrounding and in direct mechanical contact with the the first gate oxide layer and the first polysilicon layer and in direct mechanical contact with the top surface of the substrate, wherein a combined thickness of the first polysilicon layer and the first dielectric film in the first direction exceeds the thickness of the second polysilicon layer in the first direction, and wherein a combined width of the first polysilicon layer and the first dielectric film in the second direction exceeds the width of the second polysilicon layer in the second direction.

25. (Previously presented) The electrical structure of claim 24, further comprising a second dielectric film surrounding and in direct mechanical contact with the first dielectric film and in direct mechanical contact with the top surface of the substrate.

26. (Previously presented) The electrical structure of claim 25, further comprising a diffusion area in the substrate, wherein the top surface of the substrate and a top surface of the diffusion area are coplanar, and wherein the top surface of the diffusion area is in direct mechanical contact with the first gate oxide layer, the first dielectric film, and the second dielectric film.

27. (Previously presented) The electrical structure of claim 24, wherein the first dielectric film comprises silicon oxide.

28. (Previously presented) The electrical structure of claim 24, wherein the first dielectric film comprises silicon nitride.

29. (Currently amended) The electrical structure of claim 23, further comprising a dielectric cap layer on the first polysilicon layer and in direct mechanical contact with a top surface of the first polysilicon layer, and wherein the top surface of the first polysilicon layer is about parallel to the top surface ~~of~~ of the ~~subsstrate~~ substrate.

30. (Currently amended) The electrical structure of claim 29, further comprising an electrically insulative spacer in direct ~~mecanical~~ mechanical contact with the first gate oxide layer, the first polysilicon layer, and a side surface of the dielectric cap layer, and whereon a portion of the side surface of the dielectric cap layer is not in mechanical contact with the spacer.

31. (Previously presented) The electrical structure of claim 30, further comprising a diffusion area in the substrate, wherein the top surface of the substrate and a top surface of the diffusion area are coplanar, and wherein the top surface of the diffusion area is in direct mechanical contact with the first gate oxide layer and the spacer.

32. (Previously presented) The electrical structure of claim 29, wherein the dielectric cap layer comprises silicon oxide.

33. (Previously presented) The electrical structure of claim 29, wherein the dielectric cap layer

comprises silicon nitride.

34. (Previously presented) The electrical structure of claim 29, wherein the spacer comprises a silicon-rich material.

35. (Previously presented) The electrical structure of claim 34, wherein the silicon-rich material comprises silicon-rich silicon nitride.

36. (Previously presented) The electrical structure of claim 34, wherein the silicon-rich material comprises silicon-rich silicon oxynitride.

37. (Previously presented) The electrical structure of claim 23, wherein the substrate comprises single crystal silicon.

38. (Previously presented) The electrical structure of claim 23, wherein the thickness of the first gate oxide in the first direction is 3 to 5 nanometers.

39. (Canceled)

40. (Currently amended) ~~The structure of claim 39, further comprising:~~ A structure, comprising:

a semiconductor substrate;

a first gate oxide layer on the substrate and in direct mechanical contact with the top

surface of the substrate;

a first polysilicon layer on the first gate oxide layer and in direct mechanical contact with the first gate oxide layer;

an electrically insulative isolation structure within the substrate, wherein [[a]] the top surface of the substrate and a top surface of the insulation structure are coplanar;

a second gate oxide layer on the isolation structure and in direct mechanical contact with the top surface of the isolation structure; and

a second polysilicon layer on the second gate oxide layer and in direct mechanical contact with the second gate oxide layer, ~~wherein the laser beam is not directed toward the second polysilicon layer and is not adapted to trim the second polysilicon layer~~ wherein the first polysilicon layer has a smaller thickness than the second polysilicon layer in a first direction perpendicular to the top surface of the substrate, and wherein the first polysilicon layer has a smaller width than the second polysilicon layer in a second direction parallel to the top surface of the substrate.

41. (Canceled)

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

Respectfully submitted,

Jack P. Friedman

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Jack P. Friedman
Reg. No. 44,688
SCHMEISER, OLSEN & WATTS
3 Lear Jet Lane, Suite 201
Latham, N.Y. 12110
(518) 220-1850
Email: *jfriedman@iplawusa.com*